第 22 屆台灣靜電放電防護技術暨可靠度技術研討會
2024 Taiwan ESD and Reliability Conference (TESDC-2024)
議程表 Program

2024 年 10 月 30 日(三) (Wednesday, Oct. 30, 2024) -- Tutorial Day

09:00 ~ 09:10	Registration & Exhibition Open
09:10 ~ 10:40	Tutorial (A) - Part 1 Advanced ESD Basics and CDM Control for 2.5D & 3D IC *Mr. Joshua Yoo* *Core Insight, Inc.*
	Chairman: 趙傳珍
10:40 ~ 11:00	Coffee Break
11:00 ~ 12:30	Tutorial (A) - Part 2 Advanced ESD Basics and CDM Control for 2.5D & 3D IC *Mr. Joshua Yoo* *Core Insight, Inc.*
	Chairman: 趙傳珍
12:30 ~ 13:40	Lunch
13:40 ~ 15:10	Tutorial (B) - Part 1 Condition Monitoring Power Electronics for Reliability – ageing-to-failure mechanisms and characteristics *Prof. Li Ran* *University of Warwick*
	Chairman: 陳始明
15:10 ~ 15:30	Coffee Break
15:30 ~ 17:00	Tutorial (B) - Part 2 Condition Monitoring Power Electronics for Reliability – algorithms for signature extraction *Prof. Li Ran* *University of Warwick*
	Chairman: 陳始明

2024 年 10 月 31 日(四)　(Thursday, Oct. 31, 2024) -- Conference Day 1

09:20 ~ 09:30	**T-ESDA Member Registration**
09:30 ~ 09:50	**T-ESDA 第十二屆第二次會員大會**
09:50 ~ 10:00	**Coffee Break**
10:00 ~ 10:10	**TESDC-2024 Opening**
10:10 ~ 11:10	**Keynote Speech (I)** **The Influence of Gate-Series-Resistor on the ESD Protection for 650V GaN-HEMT Circuit** ***Mr. Jian-Hsing Lee*** ***Vanguard International Semiconductor Corp.***
	Chairman: 柯明道
11:10 ~ 12:10	**Invited Talk (I)** **ESD Control Challenges and Ionization Issue for Advanced Package Device** ***Mr. Joshua Yoo*** ***Core Insight, Inc.***
	Chairman: 柯明道
12:10 ~ 13:20	**Lunch** **(T-ESDA 理監事會、TESDC-2024 TPC Meeting)**
13:20 ~ 14:20	**Keynote Speech (II)** **Reliability of SiC Power Semiconductor Devices** ***Prof. Li Ran*** ***University of Warwick***
	Chairman: 吳添立
14:20 ~ 14:40	**Coffee Break**
14:40 ~ 15:40	**Invited Talk (II)** **High Current Latch Up Testing Using a Thermo Scientific MKx System** ***Mr. Marcos Hernandez*** ***Thermo Scientific***
	Chairman: 羅達權
15:40 ~ 16:00	**Coffee Break**
16:00 ~ 17:00	**Session A – ESD (I)** **New ESD Design of MV Gate-Driven NMOS without Extra Mask Cost and Process Step in 28nm Embedded High Voltage Process** **Design of a 1.8V Over Voltage Tolerant-General Purpose I/O (OVT-GPIO) Circuit Using 1.2V transistors in Samsung 4nm FinFET Technology** **Optimized Low Parasitic Capacitance ESD Clamps for High-Bandwidth 2.5D3D Chiplet Interfaces in Advanced TSMC FinFET Technology**
	Chairman: 唐天浩